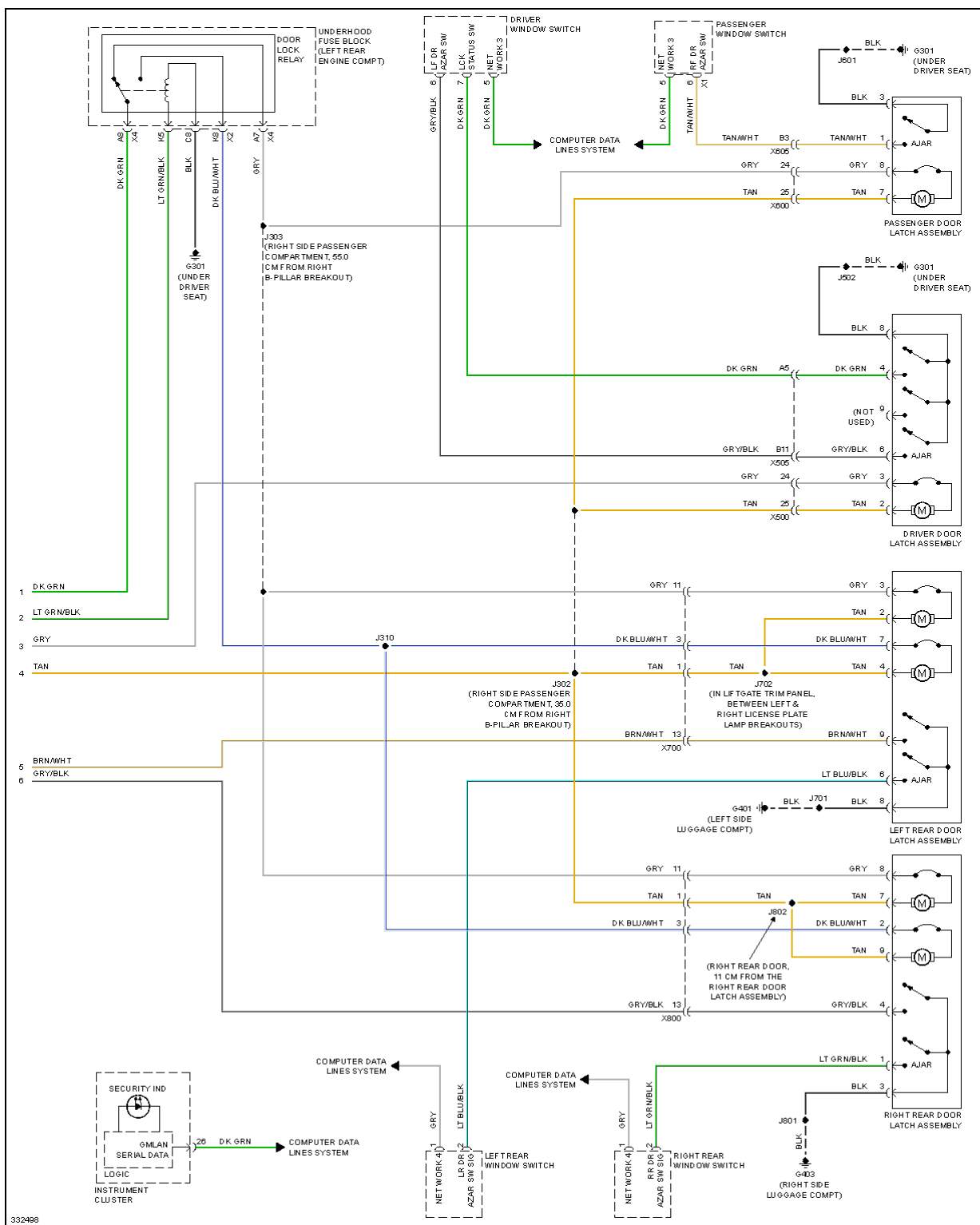



Fig. 8: Forced Entry Circuit (2 of 2)